IN THE WRITTEN SPECIFICATION:

Please amend the written specification for the above-identified patent application as follows wherein replacement paragraphs or sections are provided with deleted material is marked with a ~~strikethrough~~ and new material is underlined to show the changes made:

Please add the following paragraph to page 1, line 2:

This application claims the benefit of priority to the provisional patent application filed on 8/28/2001 having an application serial number of 60/315,867 and the provisional patent application filed on 8/28/2001 having an application serial number of 60/315,834.

Please replace the paragraph on page 3, lines 21 to 25, in the original specification with the following amended paragraph (with changes shown):

Common electrical characteristics that are extracted from an integrated circuit layout include capacitance and resistance of the various "nets" (electrical interconnects) in the integrated circuit. These electrical characteristics are sometimes referred to as "parasitic" since these ~~are~~ electrical characteristics are not intended by the designer but result from the underlying physics of the integrated circuit design.

Please replace the paragraph on page 4, lines 11 to 17, in the original specification with the following amended paragraph (with changes shown):

To test an integrated circuit layout, the parasitic resistance and parasitic capacitance are "extracted" from the integrated circuit layout and then the integrated

circuit is analyzed and possibly simulated ~~with a~~ using the extracted parasitic resistance and parasitic capacitance. If the parasitic resistance or parasitic capacitance causes ~~cause~~ undesired operation, then the integrated circuit layout must be changed. Furthermore, minimizing the amount of parasitic resistance and parasitic capacitance can optimize the performance of the integrated circuit.

Please replace the paragraph on page 6, lines 14 to 22, in the original specification with the following amended paragraph (with changes shown):

The machine learning is performed by first creating training data sets composed of the identified parameters from typical examples of the smaller extraction problem and the answers to those example extraction problems as solved using a highly accurate physics based field solver. The training data sets are then used to train the models. In one embodiment, neural networks are used to model the extraction problems. To train the neural network models, Bayesian inference is used in one embodiment. Bayesian inference may be implemented with normal Monte Carlo techniques or Hybrid Monte Carlo techniques. After the creation of a set of models for each of the smaller simpler extraction problems, the machine-learning based models may be used for extraction.

Please replace the paragraph on page 9, lines 2 to 3, in the original specification with the following amended paragraph (with changes shown):

Figure 6c illustrates the digital signal pulse of **Figure 6a** after it has been affected by parasitic capacitance.

Please replace the paragraph on page 9, lines 13 to 14, in the original specification with the following amended paragraph (with changes shown):

Figure 8B illustrates the interconnect wires of **Figure 8A** ~~**8a**~~ with a capacitance effect "halo" drawn around critical net **810**.

Please replace the paragraph on page 11, lines 2 to 3, in the original specification with the following amended paragraph (with changes shown):

Figure 19a and illustrates a four-port shape for a small resistance extraction problem. ~~The four-port extraction~~

Please replace the paragraph on page 13, lines 20 to 25, in the original specification with the following amended paragraph (with changes shown):

To extract a set of highly accurate electrical characteristics from an integrated circuit layout, an EDA extraction application may apply field solvers. Field solvers discretize the integrated circuit layout and accurately model the physical phenomena of the integrated circuit components using the known laws of physics and electromagnetism. The final output from a field solver is a highly accurate determination of the electrical characteristics of the various integrated circuit components.

Please replace the paragraph on page 14, lines 2 to 6, in the original specification with the following amended paragraph (with changes shown):

Although field solvers are very accurate, it is impractical to use field solvers to extract the electrical characteristics from an entire integrated circuit layout. Specifically, field solvers are very computationally intensive since millions of data points

must be processed. Thus, using field solvers to extract the electrical characteristics from an entire integrated circuit layout would take an unacceptable amount of time.

Please replace the paragraph on page 15, lines 9 to 16, in the original specification with the following amended paragraph (with changes shown):

Similarly, pre-calculated tables may also be used to simplify and <u>to</u> speed up the extraction of electrical characteristics from an integrated circuit layout. For example, to extract the capacitance from an interconnect net, the length of an interconnect net may first be divided into different sections wherein each section has unvarying surrounding features. Then, the known surrounding conditions for each section are used to identify an appropriate pre-calculated table that will be used to extract the capacitance. The pre-calculated tables are constructed by using a field solver for the various different surrounding condition primitives.

Please replace the paragraph on page 16, lines 2 to 10, in the original specification with the following amended paragraph (with changes shown):

Both the application of simplified formulas and pre-calculated table improve the speed of the extraction process. However, both systems achieve that increased speed by greatly sacrificing the accuracy of the extracted electrical characteristics. With the increasingly dense integrated circuits, the accuracy of extraction systems becomes very important. Specifically, as the transistors decrease in size, the transistor delay time decreases such that the effects of interconnect wire delay increases. For long interconnect wire routes, over 50% of the signal delay may be <u>caused</u> ~~cause~~ by interconnect wire delay. Thus, the importance of obtaining accurate electrical characteristics of integrated circuit designs has greatly increased.

Please replace the paragraph on page 17, lines 2 to 7, in the original specification with the following amended paragraph (with changes shown):

The system of the present invention begins by generating initial models using a first set of known training points. Experimental design techniques are then applied to the initial models to refine those models by selecting additional training data points that provide the most information. Feedback between the model generation and experimental design forces ~~force~~ the system of the present invention to converge toward a highly predictive model.

Please replace the paragraph from line 20 of page 20 to line 2 of page 21, in the original specification with the following amended paragraph (with changes shown):

Referring back to the overview diagram of **Figure 1**, once a set of extraction models has been sufficiently trained, the set of extraction models may be used for extracting electrical features from an integrated circuit design. The lower half of **Figure 1** conceptually illustrates how the set of extraction models are used for extraction. **Figure 1** will be described with reference to **Figure 3** that illustrates ~~illustrating~~ a flow diagram that describes how extraction models may be used to extract electrical features from an integrated circuit design.